

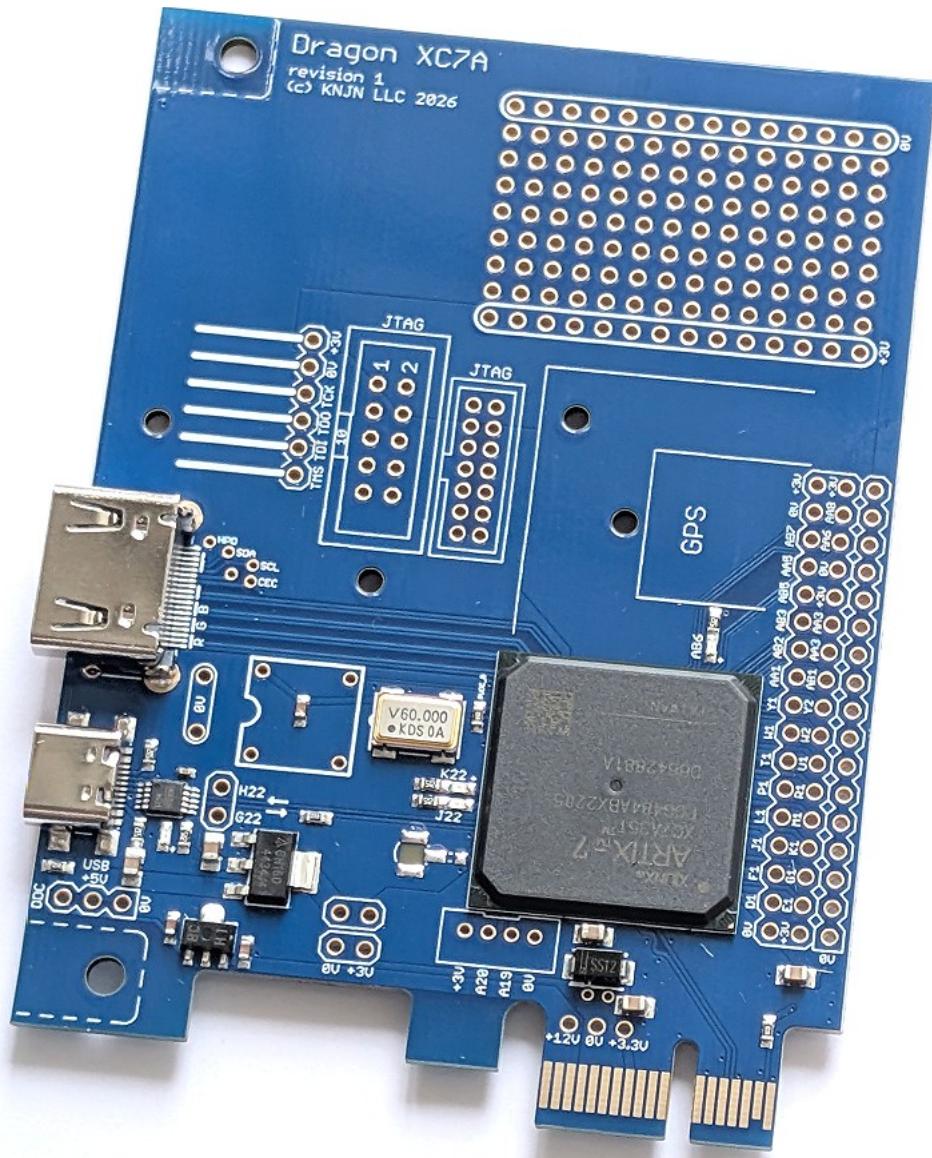
Dragon XC7A & XC7M FPGA development boards

© 2026 KNJN LLC

<https://www.knjn.com/>

This document applies to the following boards

- Dragon XC7A
- Dragon XC7M



Document last revision **February 10, 2026**

Table of Contents

| | | |
|-----|----------------------------------|----|
| 1 | Introduction..... | 4 |
| 1.1 | Features..... | 4 |
| 1.2 | FPGA configuration..... | 4 |
| 1.3 | FPGA software..... | 4 |
| 1.4 | Board power..... | 4 |
| 1.5 | Clock oscillators..... | 4 |
| 1.6 | Purchase..... | 4 |
| 2 | Vivado..... | 5 |
| 2.1 | Vivado installation..... | 5 |
| 2.2 | Vivado project..... | 5 |
| 3 | FPGAConf..... | 6 |
| 3.1 | USB driver..... | 6 |
| 3.2 | FPGA configuration..... | 6 |
| 3.3 | Boot-PROM programming..... | 6 |
| 4 | PCI Express..... | 7 |
| 5 | HDMI..... | 8 |
| 6 | High-stability clock option..... | 9 |
| 7 | Boards layout..... | 10 |
| 8 | Useful items..... | 12 |

1 Introduction

1.1 Features

- Xilinx/AMD XC7A35T FPGA
 - XC7A:
Standard height PCI express board with 30 GPIOs and 3 LEDs
High-stability clock option using a VCTCXO
 - XC7M:
Low profile PCI express board with 28 GPIOs and 3 LEDs
- HDMI output
- USB-C with CH340 serial interface

1.2 FPGA configuration

The FPGA is configured using either a Xilinx/AMD or KNJN JTAG cable.

- Xilinx/AMD: use a [DLC10](#) or compatible cable.
- KNJN: use the KNJN JTAG cable for Dragon XC7A & XC7M ([KNJN item#5179](#))

1.3 FPGA software

Download and install the latest [Vivado](#) software. When using the KNJN JTAG cable, we also provide [FPGAconf](#).

1.4 Board power

The board can be powered in multiple ways.

1. PCI express
2. USB-C
3. KNJN JTAG cable
4. External lab power supply, either 3.3V or 5V

1.5 Clock oscillators

The boards support DIL-8, SMD 5x7 and SMD3225 clock oscillators to drive different FPGA clock inputs.

| Board | DIL-8 | SMD 5x7 | SMD3225 |
|------------|-----------|-----------|-----------|
| XC7A | To solder | 60MHz | To solder |
| XC7M rev 1 | To solder | To solder | To solder |
| XC7M rev 2 | To solder | To solder | 25MHz |

Other clock sources include the PCI express interface and the internal configuration clock. Check the LEDglow source code example for more details.

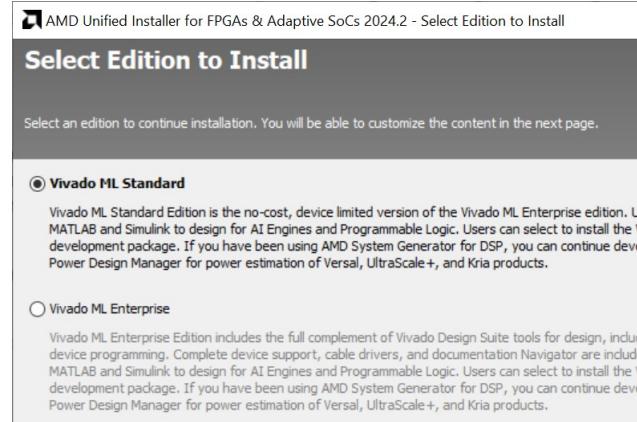
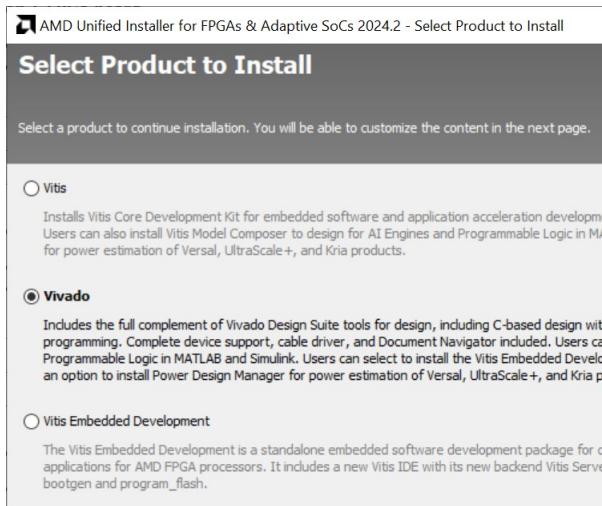
1.6 Purchase

Want one? Go to KNJN's [PCI FPGA development boards](#) shopping page.

2 Vivado

2.1 Vivado installation

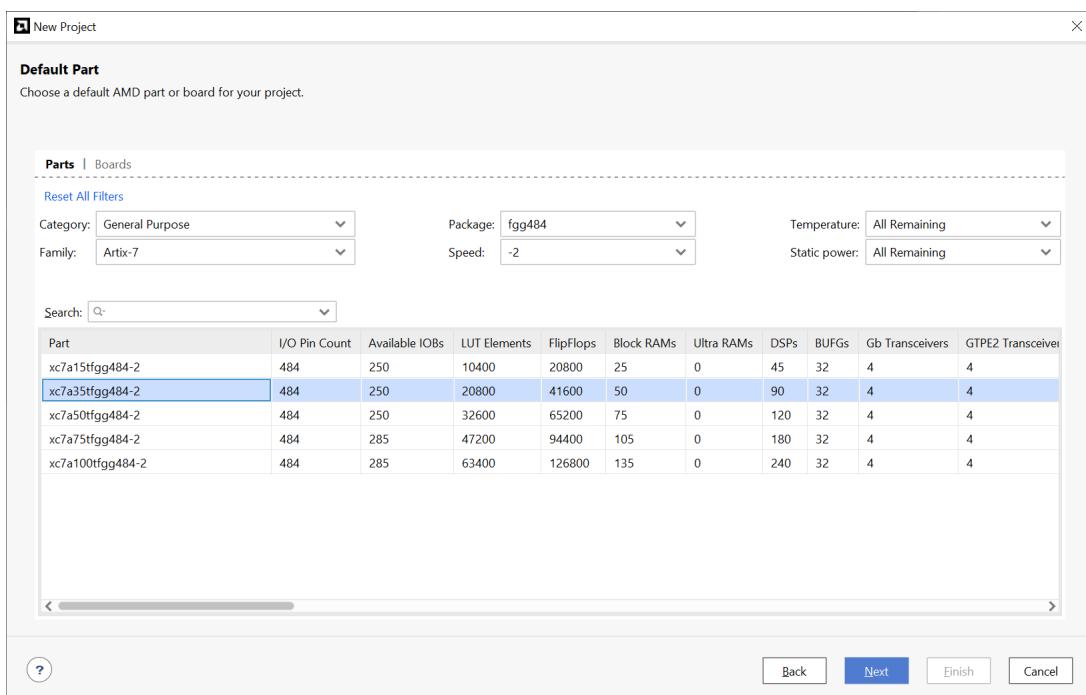
Download and install the free version of [Vivado](#)



2.2 Vivado project

Once Vivado is installed, you are ready to create a new FPGA project.

Select the XC7A35T in FGG484 package.



3 FPGACONF

FPGACONF is a software used with the KNJN JTAG cable for FPGA configuration and boot-PROM programming.

3.1 USB driver

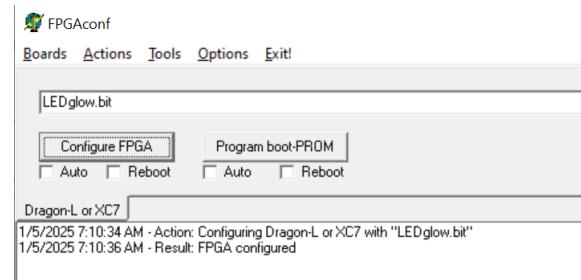
The “KNJN JTAG cable” is provided with a USB driver. The driver is signed and compatible with Windows 10/11.

1. Plug-in the KNJN JTAG cable in your PC’s USB port.
2. Go to the Device Manager and find the new unrecognized device in the USB section. Click on “Update Driver” and select the driver folder.

3.2 FPGA configuration

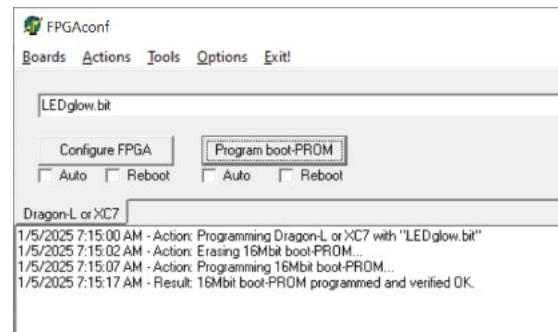
Run FPGACONF.

In the “Boards” menu, select “Dragon-L or XC7 (JTAG)”. Then select a bitfile and click on “Configure FPGA”.



3.3 Boot-PROM programming

Select a bitfile and click on “Program boot-PROM”.



4 PCI Express

The simplest way to get started is with the PIO example.

<https://www.youtube.com/watch?v=1YgvjyNfLYY>

1. Create a PIO example project with a XC7A35TFFG484-2

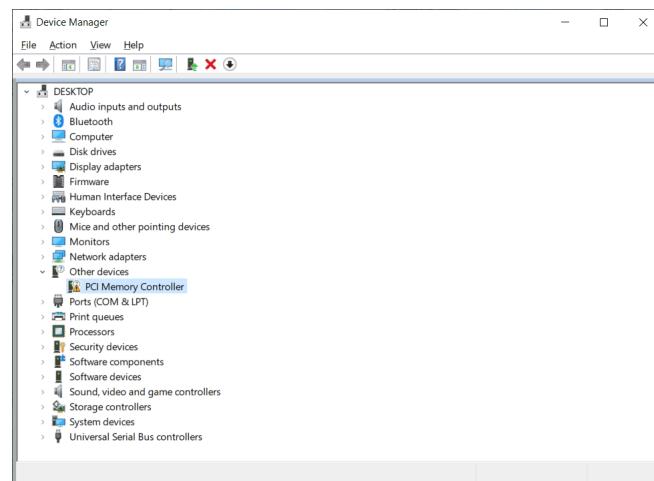
2. Add these lines to the XDC file

```
set_property PACKAGE_PIN A8 [get_ports pci_exp_rxn[0]]
set_property PACKAGE_PIN A4 [get_ports pci_exp_txn[0]]
set_property CFGBVS VCCO [current_design]
set_property CONFIG_VOLTAGE 3.3 [current_design]
set_property BITSTREAM.GENERAL.COMPRESS true [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN pullup [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 2 [current_design]
set_property BITSTREAM.CONFIG.CONFIGRATE 50 [current_design]
```

and compile the design to get a bit file.

3. Program the bit file in the boot-PROM.

4. Insert the Dragon board into a PCI express socket of your test PC (while the PC is un-powered). Boot the test PC. The board should be recognized by your OS.



5 HDMI

The HDMI source code is a port from <https://github.com/hdl-util/hdmi>

6 High-stability clock option

If a high-stability clock is desired, the XC7A board can be fitted with a VCTCXO. These oscillators are quite stable, with a typical stability of $\pm 2.5\text{ppm}$.

Then a GPS module can be used to monitor the VCTCXO output and create a GPSDO.

1. Solder a SMD3225 (or smaller SMD2520) VCTCXO on the board, like a [RTV-104EF13P-S-10.000-TR](#) or [TG2520SMN 40.0000M-CCGNDM5](#)

The SMD3225 oscillator footprint is located below the FPGA on the back of the board.

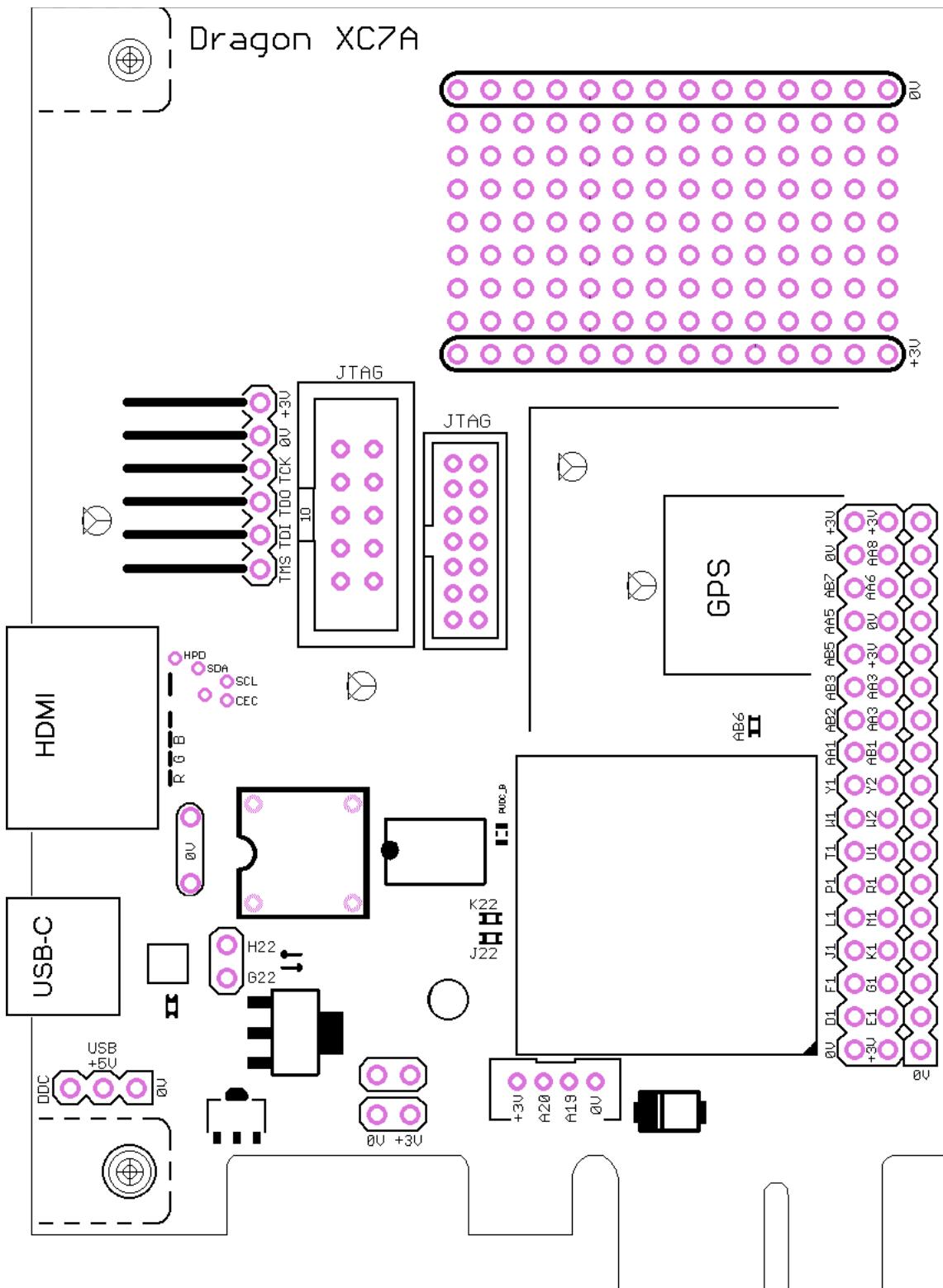
2. Connect a GPS module to the space marked “GPS” on the board.

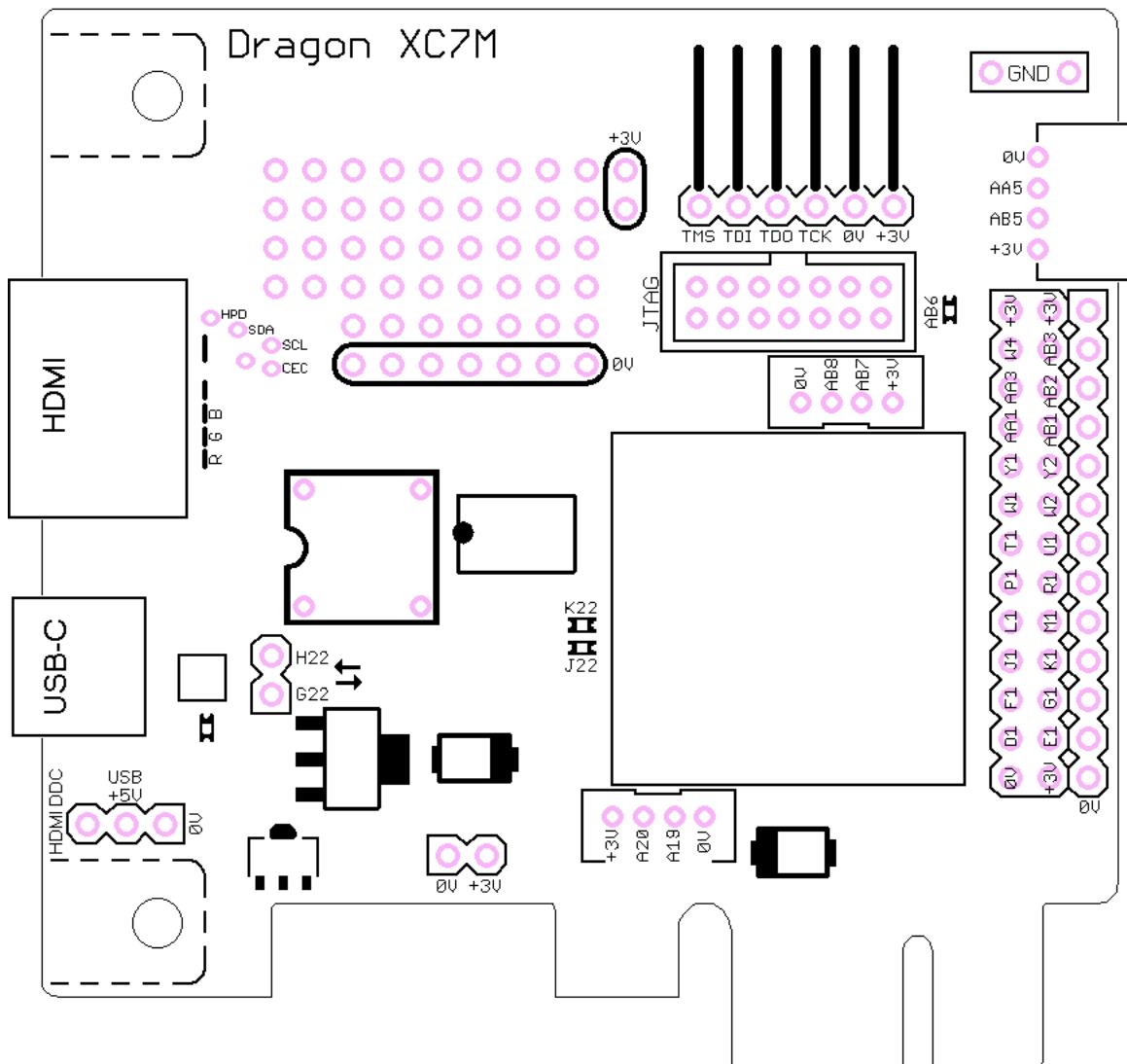
Make sure to use a GPS module with PPS output. These modules have five pins (usually VCC, GND, RxD, TxD and PPS) and can be powered with either 3.3V or 5V.

Now run the GPSDO example code.

You can order the XC7A board with a VCTCXO and GPS from the [FPGA kits](#) page.

7 Boards layout





Notice the IOs indicated on the header pins.

Check also “Dragon XC7M IO schematic.pdf” in the board’s startup-kit.

8 Useful items

| Item name | item# |
|---|---------------------------|
| KNJN USB JTAG cable for Dragon XC7A & XC7M | 5179 |
| Xilinx style JTAG 2x7 shrouded connector for use with DLC10 | 2189 |
| DIL-8 oscillator socket | 2187 |
| Oscillators DIL-8 or SMD5x7 | 7000~7999 |